UCS512A Specification

Description

UCS512A is the DMX512 differential parallel protocol LED driver chip, the 1/2/3 channel constant current output are optional, the UCS512A decoding technology decoding DMX512 signal accurately, UCS512A can auto-decode DMX512 signal that transmission frequency is within 200K-500K without any speed settings,addressing up to 4096 channels. UCS512A include E2PROM and support online writing code, One-time online writing code can finish 100 meters (spacing) *1024 (cascaded UCS512A points). The chips including 4*60ma constant current output port whose pressure value is above 24V. it have externeral resitor to adjust current. it have PWM reverse polarity and reducing-frequency output function, this function is suitable to texternal triode, MOS diode or a high current drive IC using.the chips' port is with high fresh rate to improve screen image quality.

It is mainly for building decoration and stage lighting LED lighting system , abnormal chip does not affect other normal chips working, maintenance is simple and convenient.

Feature

1. Compatible withDMX512 (1990) signaling protocol;

2.Control mode: DMX512 differentinal Signal in parallel, maximum support 4096 channel

3.Exclusive adaptive decoding technology, Auto-decode DMX512 signaltransmission rate of 200K ~500kbps.

4. E2PROM built in chips

5. it include receiving 485 signal modules. it can recognize the 485 signal accurately and high diffrentnial impedance to impove load capacity greatly.

6. one series writting line can write code one time for all channel.

7.Enhanced online cascade writting code mode, support 100 meters (spacing) *1024 (cascaded UCS512A points) one-time online writing code

8.PWM control unit correct 256 gray level as 1024 gray level gamma correction .

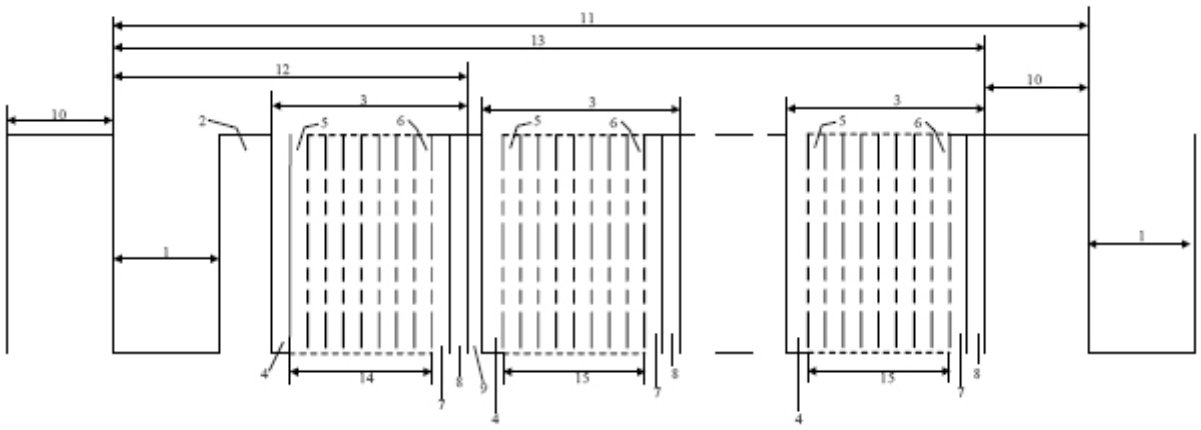
9. RGB 3 chanel output, Max 60mA /Channel

10. External resistor can adjust currect from 3mA/CH to 60mA/CH

11. power on self test (white color), writting code finishing (Blue color)

12. The 80nS output channel delay, reducing the surge current interference.

Data Transmission Protocol



Figuer Key

1- "SPACE" for BREAK
2- "MARK" After BREAK (MAB)
3- Slot Time
4- START Bit
5- LEAST SIGNIFICANT Data BIT
6- MOST SIGNIFICANT Data BIT
7- STOP Bit
8- STOP Bit
9- "MARK" Time Between slots
10- "MARK" Before BREAK (MBB)
11- BREAK to BREAK Time
12- RESET Sequence (BREAK,MAB,START Code)
13- DMX512 Packet
14- START CODE (Slot 0 Data)
15- SLOT 1 DATA
16- SLOT nnn DATA (Maximun 512)

Designation	Description	Min	Typical	Max	Unit
-	Bit Rate	245	250	255	kbit/s
-	Bit Time	3.92	4	4.08	us
-	Minimum Update Time for 513 slots	-	22.7	-	ms
-	Maximum Update Rate for 513 slots	-	44	-	/s
1	"SPACE" for BREAK	88	-	-	us
2	"MARK" After BREAK (MAB)	8	-	 <1.00	us s
9	"MARK" Time Between slots	0	-	<1.00	s
10	"MARK" Before BREAK (MBB)	0	-	<1.00	s
11	BREAK to BREAK Time	1196	-	 1.00	us s
13	DMX512 Packet	1196	-	 1.00	us s